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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,201	03/12/2004	Jeoung-Mo Koo	8021-205 (SS-17942-US)	7424

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/799,201	KOO ET AL.
	Examiner	Art Unit
	Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-17 filed June 15, 2005 is acknowledged. The traversal is on the ground that search and examination of the whole application can be done without serious burden. This is not found persuasive because the invention of Group I, claims 1-17 are drawn to an integrated circuit, classified in class 257, subclass 314, while the invention of Group II, claims 18-23 are drawn to a method of fabricating an integrated circuit, classified in class 438, subclass +1. They are shown to be different inventions and having a separate status in the art by their different classifications. The requirement is still deemed proper and is therefore made **FINAL.**

Drawings

2. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are, not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2, 9, 16 objected to because of the following informalities: Claim 2 includes the limitation "*a source region and a drain region formed in the active area at least one of under and adjacent both sides of the control gate*". Claim 9, includes the limitations "*a first source region and a first drain region formed in the active area at least one of under and adjacent both sides of the first gate*" and "*a second source region and a second drain region formed in the active area at least one of under and adjacent both sides of the second gate*". Claim 16 includes the limitations "*a first source region and a first drain region formed in the second area at least one of under and adjacent both sides of the first gate*" and "*a second source region and a second drain region formed in the third area at least one of under and adjacent both sides of the second gate*". However, the phrase "at least one of" implies **either** condition of "at least under" or "adjacent both sides" when referring to the source and drain regions in relation to the control gate of the first and second gates; and the term "and" implies **both** of the aforementioned conditions.

The examiner suggests amending said claims to include the phrase "*at least one of under **or** adjacent*", in order to avoid confusion as to the relation between the active regions and the gates.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art as disclosed on prior art figures 1-3 and their description of pages 1-2 of the instant application. With regard to Claim 1, Applicant's admitted prior art discloses on figure 2 a one-time programmable memory device (page 1, lines 21-25 of the instant application), comprising:

an isolation layer (5) for defining an active area containing source (60) and drain (65) regions, thus providing the claimed active region;

an oxide layer (15) formed on the active area;

a floating gate (20) formed over the active area and the isolation layer (5);

an inter-gate dielectric layer (40) formed on formed on the floating gate (20);

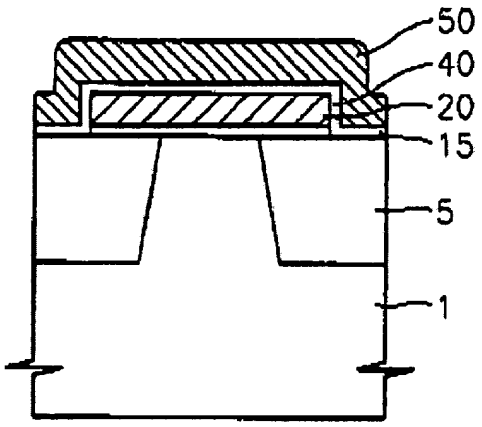
and a control gate (50) formed on the inter-gate dielectric layer (40).

With regard to Claim 2, Applicant's admitted prior art discloses a source region (60) and a drain region (65) formed in the active area at least one of under and adjacent both sides of the control gate (figure 2).

With regard to Claim 4, Applicant's admitted prior art discloses control gate (50) is formed over the floating gate (20). See figure 2.

With regard to Claim 5, Applicant's admitted prior art discloses a control gate (50) that is formed so as to enclose at least one sidewall of the floating gate (20). See figure 3.

FIG. 3



5. Claims 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsubara (U.S. Patent No. 6,037,625). With regard to Claim 9, Matsubara discloses (column 1, lines 7-18 and figure 2K) an integrated circuit, comprising:

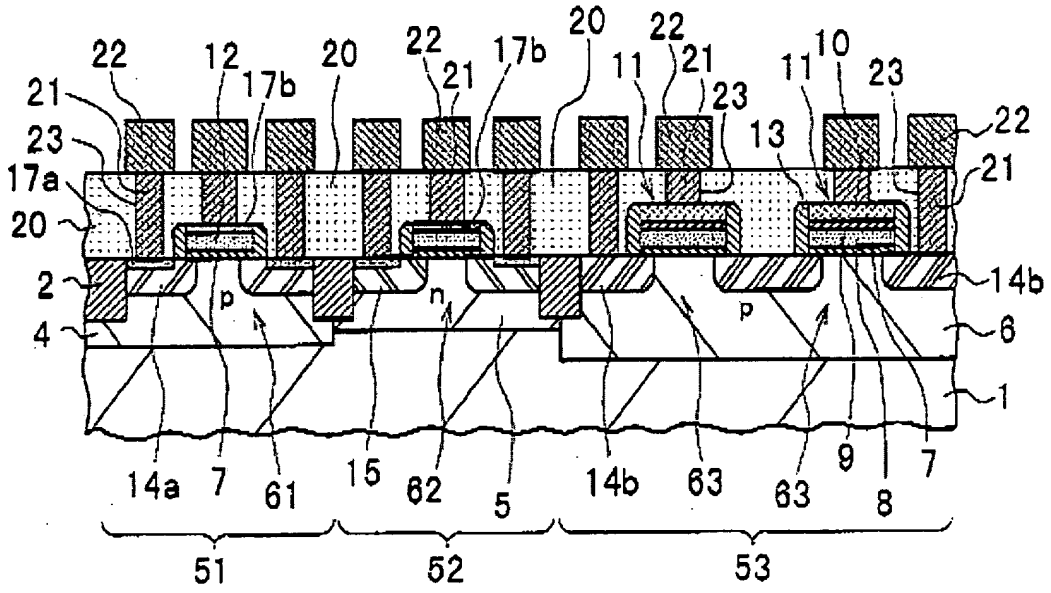
a memory device (region 53 column 9, line 2) including an isolation layer (2) which comprises an STI layer and defines an active area including source/drain regions (14b) of a substrate (1), a tunnel oxide layer (7), a floating gate (8) formed over the active area of the memory device and the isolation layer (2), inter-gate dielectric layer (9) formed on the floating gate (8), and a control gate (10) formed on the inter-gate dielectric layer (9);

a first transistor (see region 51) including a first gate (12), a first gate oxide layer (7) interposed between the first gate (12) and the substrate (1), the first source/drain regions (14a)

are formed in the active area at least one of under and adjacent both sides of the first gate (12); and

a second transistor (see region 52) including a second gate (also labeled 12), a second gate oxide layer (also labeled 7) interposed between the second gate and the substrate (1) and second source/drain regions (15) are formed in the active area at least one of under and adjacent both sides of the first gate (also labeled 12).

FIG. 2K



With regard to Claim 10, Matsubara discloses a memory device (region 53) including source/drain regions (14b) formed in an active area at least one of under and adjacent both sides of the control gate (10).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as disclosed on figures 1-3 and pages 1-2 of the instant application in view of Hsu (U.S. Patent Application Publication 2005/0074935). With regard to Claim 3, Applicant's admitted prior art essentially discloses the claimed invention but fails to disclose the claimed portion of the floating gate formed over the active area that is narrower than a portion of the floating gate formed over the isolation layer. However, Hsu discloses (figure 2) a memory cell (200), which includes a floating gate (216) having a portion over an active region defined by source region (211) and drain region (212) that is narrower than the portion of the floating gate that is not over the active region, namely the portion outside region (202).

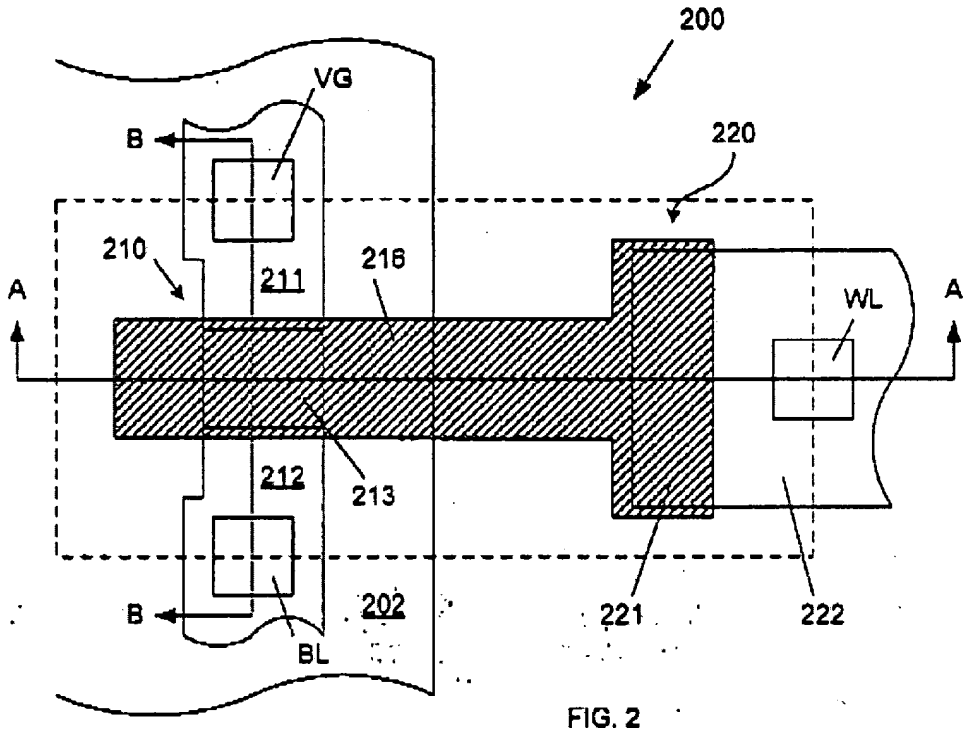


FIG. 2

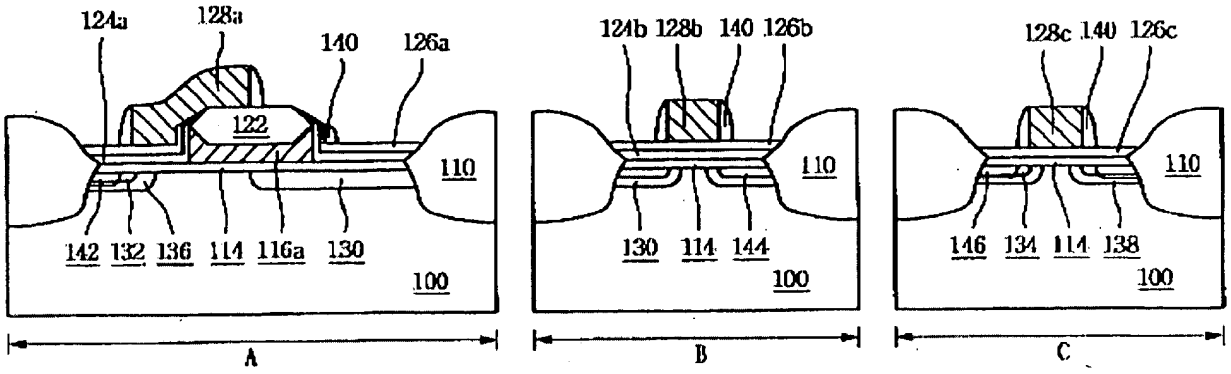
Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed portion of the floating gate formed over the active area that is narrower than a portion of the floating gate formed over the isolation layer, as suggested by Hsu, in order to facilitate the formation of a contact hole to the floating gate by forming said contact hole in the wider portion.

7. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as disclosed on figures 1-3 and pages 1-2 of the instant application in view of Matsubara (U.S. Patent No. 6,037,625). With regard to Claims 6-8, Applicant's admitted prior art essentially discloses the claimed invention but fails to disclose, the claimed inter-gate dielectric layer including a silicon nitride layer. However, Matsubara discloses an inter-gate dielectric layer (9) that is made from layer (39), and as shown on figures 2D and 2E, which is a

ONO layer formed by threes stacked sub-films comprising a SiO2 sub-film, a Si3N4 sub-film and a SiO2 sub-film (column 9, lines 20-22). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed inter-gate dielectric layer including a silicon nitride layer, a composite layer having a silicon nitride layer or a silicon oxide layer or a composite layer having a silicon oxide layer, silicon nitride layer and a silicon oxide layer, known also as ONO, as suggested by Matsubara, in order to provide a storage dielectric material with a higher dielectric constant than silicon oxide that can prevent electric charges accumulated in the floating gate to leak during a writing process.

8. Claims 11, 14 -16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara et al. (U.S. Patent No. 6,037, 625) in view of Lee (U.S. Patent No. 6,348,378). With regard to Claim 11, Matsubara essentially discloses the claimed invention but fails to disclose the claimed second gate oxide layer being thinner than the first gate oxide layer. However, Lee discloses a semiconductor device including a memory device (region A of substrate 100) and transistors (defined by regions B and C of substrate 100), wherein the gate oxide (defined by layers 114 and 126b) of the transistor of region C is thinner than the gate oxide (defined by layers 114, 124b, 126c) of the transistor of region B, as clearly shown on figure 16 and included herein.

FIG. 16



Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara to include the claimed second gate oxide layer being thinner than the first gate oxide layer, as suggested by Lee, in order to provide gate oxide layers with different thickness for high and low voltage transistors (column 9, lines 65-67 and column 10, lines 1-4).

With regard to Claim 14, Matsubara discloses a second gate oxide layer (7) of the second transistor (defined by region 52 of substrate 1) having the same thickness as the tunnel oxide layer (also labeled 7) of the memory device (defined by region 53), refer to figures 2D and 2E which show the formation of oxide film (7) having the same thickness for the portion acting as gate oxide for the transistors of regions (51 and 52) and as tunnel oxide for the memory device of region 53.

Matsubara fails to disclose the claimed first gate oxide layer being thicker than the tunnel oxide and the second gate oxide layer. However, Lee discloses a semiconductor device including a memory device (region A of substrate 100) and transistors (defined by regions B and C of substrate 100), wherein the gate oxide (defined by layers 114, 124b, 126c) of the transistor of region B is thicker than the gate oxide (defined by layers 114 and 126c) of the transistor of region C and the tunnel oxide (defined by layers 124a and 126a) of the memory device of region A.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara to include the claimed first gate oxide layer being thicker than the tunnel oxide and the second gate oxide layer, as suggested by Lee, in order to provide a gate oxide layer with a suitable thickness for a high voltage transistor (column 9, lines 65-67 and column 10, lines 1-4).

With regard to Claim 15, a further difference between the claimed invention and Matsubara is, the claimed first and second gates formed form the same material as the control gate. However, Lee discloses a control gate (128a), a first gate (128b) and a second gate (128b), wherein all three gates are made from the same material (column 10, lines 6-13). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara to include the claimed first and second gates formed from the same material as the control gate, as suggested by Lee, in order to simplify the manufacturing process by using a single material for the first and second gates as well as the control gate.

With regard to Claim 16, Matsubara discloses on figure 2K an integrated circuit, comprising:

a plurality of isolation layers (2) for defining a first area (53), a second area (51) and a third area (52) in a substrate (1);

a memory device (see region 53) including a floating gate (8) formed over the first area (53) and at least one isolation layer of the plurality of isolation layers (2), an inter-gate dielectric (9) made from layer (39), as shown on figures 2D and 2E, and that includes a composite having a silicon oxide layer and a silicon nitride layer (column 9, lines 20-22) and a control gate (10) formed on the inter-gate dielectric layer (9);

a first transistor (see region 51) including a first gate (12), wherein the first gate (12) is formed in the second area (51) of the substrate on a first gate oxide layer (7) having a thickness equal to a thickness of a tunnel oxide (also labeled 7) formed on the substrate (1) for the memory device (defined by region 53), and a first source region and first drain region (both labeled 14b) formed in the second area (51) at least one under and adjacent both sides of the first gate (12); and

a second transistor (see region 52) including a second gate (also labeled 12), wherein the second gate is formed on a second gate oxide layer (also labeled 7), and a second source region and second drain region (also labeled 14b) formed in the third area (52) at least one of under and adjacent both sides of the second gate (also labeled 7).

Matsubara fails to disclose the claimed first and second gates formed of the same material as the control gate and the claimed second gate oxide layer being thinner than the first gate oxide layer. However, Lee discloses a control gate (128a), a first gate (128b) and a second gate (128b),

wherein all three gates are made from the same material (column 10, lines 6-13). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara to include the claimed first and second gates formed form the same material as the control gate, as suggested by Lee, in order to simplify the manufacturing process by using a single material for the first and second gates as well as the control gate.

Regarding the claimed second gate oxide layer being thinner than the first gate oxide layer, Lee discloses a semiconductor device including a memory device (region A of substrate 100) and transistors (defined by regions B and C of substrate 100), wherein the gate oxide (defined by layers 114 and 126c) of the transistor of region C is thinner than the gate oxide (defined by layers 114, 124b, 126c) of the transistor of region B, as clearly shown on figure 16 and included herein.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara to include the claimed second gate oxide layer being thinner than the first gate oxide layer, as suggested by Lee, in order to provide gate oxide layers with different thickness for high and low voltage transistors (column 9, lines 65-67 and column 10, lines 1-4).

9. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara et al. (U.S. Patent No. 6,037, 625) in view of Furuhata et al. (U.S. Patent No. 6,429,073). With regard to Claim 12, Matsubara essentially discloses the claimed invention but

fails to show the claimed the second gate oxide layer thinner than the tunnel oxide layer, and the first gate oxide layer thicker than the tunnel oxide layer and the second gate oxide layer. However, Furuhata discloses a first gate oxide layer (22) made from a layer (22aL) being thicker (column 12, lines 39-41) than a tunnel oxide (26), which has a thinner thickness (column 10, 53-55) and a second gate oxide (20) which can have a thickness less than or equal to a thickness of a tunnel oxide layer (26), since the thickness (3-13 nm, column 7, lines 39-42) of the second gate oxide layer (20) can be set to be less or equal to the thickness (6-9 nm, column 6, lines 53-56) of the tunnel oxide layer.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara to include the claimed invention but fails to show the claimed the second gate oxide layer thinner than the tunnel oxide layer, and the first gate oxide layer thicker than the tunnel oxide layer and the second gate oxide layer, as suggested by Furuhata, in order to provide a tunnel oxide layer with a thickness based on the functionality of the memory device and gate oxide layers for transistors with different voltage requirements.

With regard to Claim 13, a further difference between the claimed invention and Matsubara is, the claimed first and second gate formed of the same material as the control gate. However, Furuhata discloses (column 13, lines 9-15) forming gate electrodes for each of the memory transistor (400) and the voltage-type transistors (100, 200 and 300) using the material (polysilicon).

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara et al. (U.S. Patent No. 6,037, 625) in view of Lee (U.S. Patent No. 6,348,378) and further in view of Hsu (U.S. Patent Application Publication 2005/0074935). With regard to Claim 17, Matsubara and Lee essentially disclose the claimed invention but fail to disclose the claimed portion of the floating gate formed over the active area that is narrower than a portion of the floating gate formed over the isolation layer.

However, Hsu discloses (figure 2) a memory cell (200), which includes a floating gate (216) having a portion over an active region defined by source region (211) and drain region (212) that is narrower than the portion of the floating gate (216) that is not over the active region.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Matsubara and Lee to include the claimed portion of the floating gate formed over the active area that is narrower than a portion of the floating gate formed over the isolation layer, as suggested by Hsu, in order to facilitate the formation of a contact hole to the floating gate by forming said contact hole in the wider portion.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
6/22/05

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